a silicate interface layer formed over the substrate; and

a high-k dielectric layer formed over the silicate interface layer;

a gate formed over the high-k dielectric layer; and

a source/drain region formed adjacent the gate.

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45. (Amended) A capacitor for a semiconductor device, comprising;

a lower electrode;

a silicate interface layer formed over the lower electrode;

a high-k dielectric layer formed over the silicate interface layer; and

an upper electrode formed over the high-k dielectric layer.
